OKI Semiconductor

This version: Jan. 1998
Previous version: Aug. 1996

MSM81C55-5RS/GS/JS

2048-Bit CMOS STATIC RAM WITH I/O PORTS AND TIMER

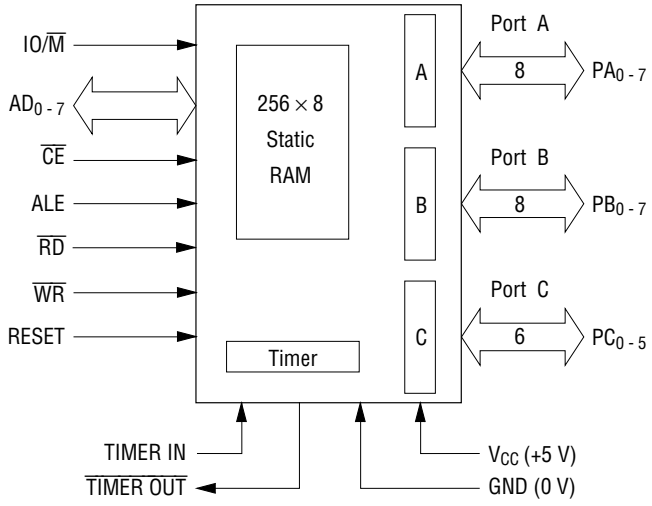
GENERAL DESCRIPTION

The MSM81C55-5 has a 2k-bit static RAM (256 bytes) with parallel I/O ports and a timer. It uses silicon gate CMOS technology and consumes a standby current of 100 micro ampere, maximum, while the chip is not selected. Featureing a maximum access time of 400 ns, the MSM81C55-5 can be used in an MSM80C85AH system without using wait states. The parallel I/O consists of two 8-bit ports and one 6-bit port (both general purpose).
The MSM81C55-5 also contains a 14-bit programmable counter/timer which may be used for sequence-wave generation or terminal count-pulsing.

FEATURES

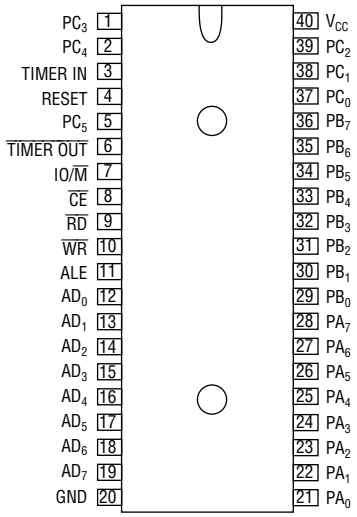
- High speed and low power achieved with silicon gate CMOS technology
- 256 words x 8bits RAM
- Single power supply, 3 to 6 V
- Completely static operation
- On-chip address latch
- 8-bit programmable I/O ports (port A and B)
- TTL Compatible
- RAM data hold characteristic at 2 V
- 6-bit programmable I/O port (port C)
- 14-bit programmable binary counter/timer
- Multiplexed address/data bus
- Direct interface with MSM80C85AH
- 40-pin Plastic DIP (DIP40-P-600-2.54): (Product name: MSM81C55-5RS)
- 44-pin Plastic QFJ (QFJ44-P-S650-1.27): (Product name: MSM81C55-5JS)
- 44-pin Plastic QFP (QFP44-P-910-0.80-2K): (Product name: MSM81C55-5GS-2K)

FUNCTIONAL BLOCK DIAGRAM

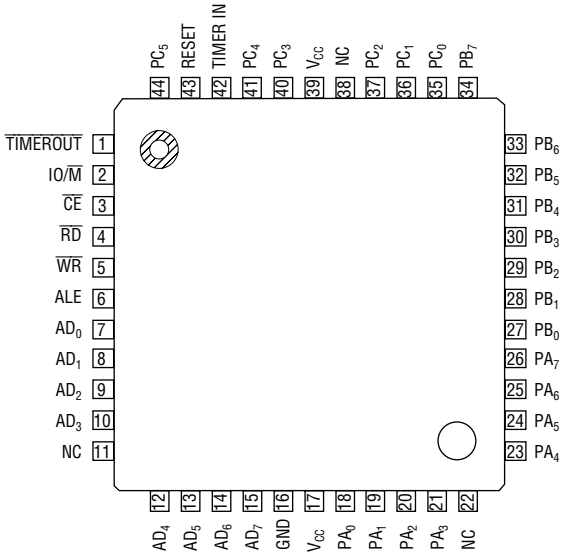


PIN CONFIGURATION (TOP VIEW)

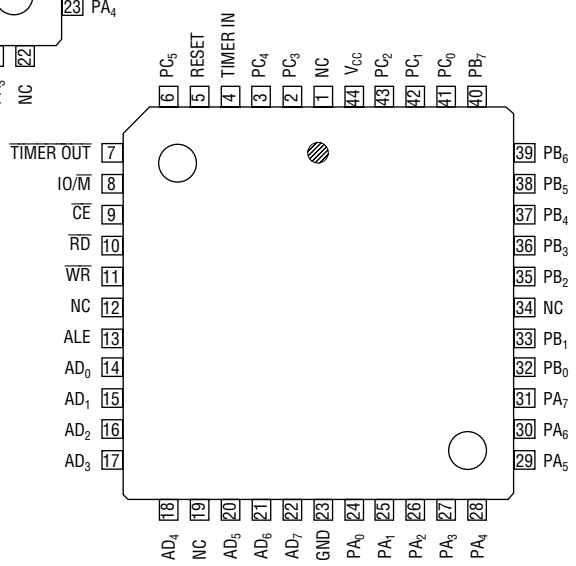
40 pin Plastic DIP



44 pin Plastic QFP



44 pin Plastic QFJ



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Conditions	Rating			Unit
			MSM81C55-5RS	MSM81C55-5GS	MSM81C55-5JS	
Power Supply Voltage	V_{CC}	Referenced to GND	–0.5 to +7			V
Input Voltage	V_{IN}		–0.5 to V_{CC} +0.5			V
Output Voltage	V_{OUT}		–0.5 to V_{CC} +0.5			V
Storage Temperature	T_{STG}	—	–55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING CONDITION

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	–40 to +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (81C55)	V_{CC}	4.5	5	5.5	V
Operating Temperature (81C55)	T_{OP}	–40	+25	+85	°C
"L" Level Input	V_{IL}	–0.3	—	+0.8	V
"H" Level Input	V_{IH}	2.2	—	V_{CC} +0.3	V
Supply Voltage (81C55-5)	V_{CC}	4.75	5	5.25	V
Operating Temperature (81C55-5)	V_{OP}	–40	+25	+70	°C

DC CHARACTERISTICS

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
"L" Level Output Voltage	V_{OL}	I_{OL} = 2 mA	V_{CC} = 4.5 V to 5.5 V Ta = –40°C to 85°C	—	—	0.45	V
"H" Level Output Voltage	V_{OH}	I_{OH} = –400 µA		2.4	—	—	V
		I_{OH} = –40 µA		4.2	—	—	V
Input Leak Current	I_{LI}	$0 \leqq V_{IN} \leqq V_{CC}$		–10	—	10	µA
Output Leak Current	I_{LO}	$0 \leqq V_{OUT} \leqq V_{CC}$		–10	—	10	µA
Standby Current	I_{CCS}	$\overline{CE} \geqq V_{CC}$ –0.2 V $V_{IH} \geqq V_{CC}$ –0.2 V $V_{IL} \leqq$ –0.2 V		—	0.1	100	µA
Mean Operating Current	I_{CC}	Memory cycle time: 1 µs		—	—	5	µA

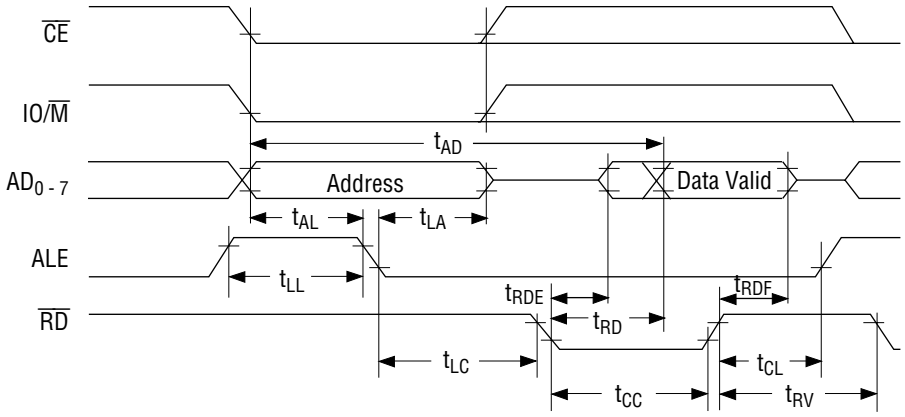
AC CHARACTERISTICS

Parameter	Symbol	V_{CC} = 4.5 V to 5.5 V, Ta = –40 to +80°C 80C85AH 3MHz I/F		V_{CC} = 4.75 V to 5.25 V, Ta = –40 to +70°C 80C85AH 5MHz I/F		Unit	Remarks
		Min.	Max.	Min.	Max.		
Address/latch Setup Time	t_{AL}	50	—	37	—	ns	
Latch/address Holt Time	t_{LA}	30	—	30	—	ns	
Latch/read (write) Delay Time	t_{LC}	100	—	40	—	ns	
Read/output Delay Time	t_{RD}	—	170	—	140	ns	
Address/output Delay Time	t_{AD}	—	400	—	330	ns	
Latch Width	t_{LL}	100	—	70	—	ns	
Read/data Bus Floating Time	t_{RDF}	0	100	0	80	ns	
Read (write)/latch Delay Time	t_{CL}	20	—	20	—	ns	
Read (write) Width	t_{CC}	250	—	200	—	ns	
Data In/write Setup Time	t_{DW}	150	—	100	—	ns	
Write/data-in Hold Time	t_{WD}	0	—	25	—	ns	
Recovery Time	t_{RV}	300	—	200	—	ns	
Write/port Output Delay Time	t_{WP}	—	400	—	300	ns	
Port Input/read Setup Time	t_{PR}	70	—	50	—	ns	Load capacitance: 150 pF
Read/port Input Hold Time	t_{RP}	50	—	10	—	ns	
Strobe/buffer Full Delay Time	t_{SBF}	—	400	—	300	ns	
Strobe Width	t_{SS}	200	—	150	—	ns	
Strobe/buffer Empty Delay Time	t_{RBE}	—	400	—	300	ns	
Strobe/interrupt-on Delay Time	t_{SI}	—	400	—	300	ns	
Read/interrupt-off Delay Time	t_{RDI}	—	400	—	300	ns	
Port Input/strobe Setup Time	t_{PSS}	50	—	20	—	ns	
Strobe/port-input Hold Time	t_{PHS}	120	—	100	—	ns	
Strobe/buffer-empty Delay Time	t_{SBE}	—	400	—	300	ns	
Write/buffer-full Delay Time	t_{WBF}	—	400	—	300	ns	
Write/interrupt-off Delay Time	t_{WI}	—	400	—	300	ns	
Time Output Delay Time Low	t_{TL}	—	400	—	300	ns	
Time Output Delay Time High	t_{TH}	—	400	—	300	ns	
Read/data Buse Enable Delay Time	t_{RDE}	10	—	10	—	ns	
Timer Cycle Time	t_{CYC}	320	—	320	—	ns	
Timer Input Rise and Fall Times	t_r, t_f	—	80	—	80	ns	
Timer Input Low Level Time	t_1	80	—	40	—	ns	
Timer Input High Level Time	t_2	120	—	70	—	ns	
WRITE to TIMER-IN for writes which start counting	t_{WT}	200	—	200	—	ns	
TIMER-IN to WRITE for writes which start counting	t_{TW}	0	—	0	—	ns	

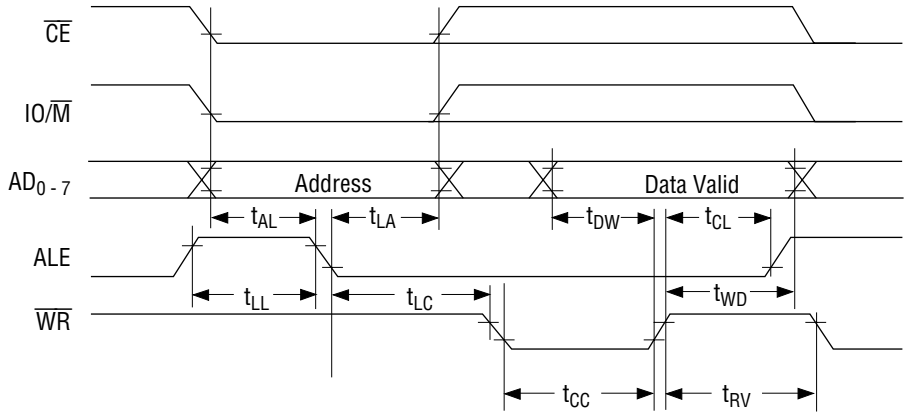
Note: Timings are measured wth V_L = 0.8 V and V_H = 2.2 V for both input and output.

TIMING DIAGRAM

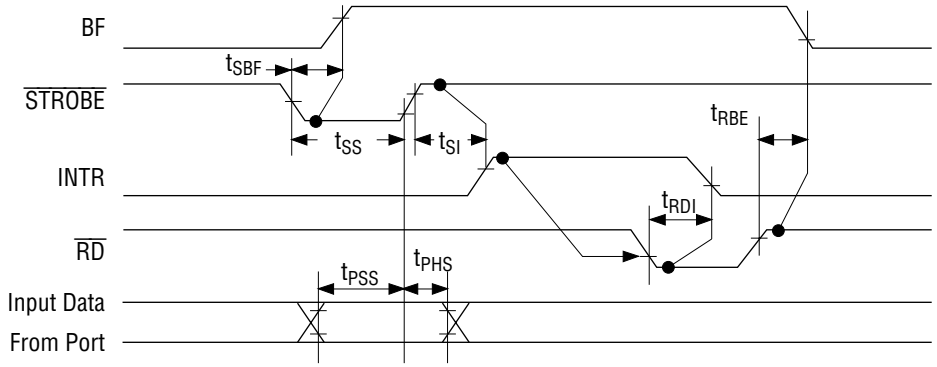
Read Cycle



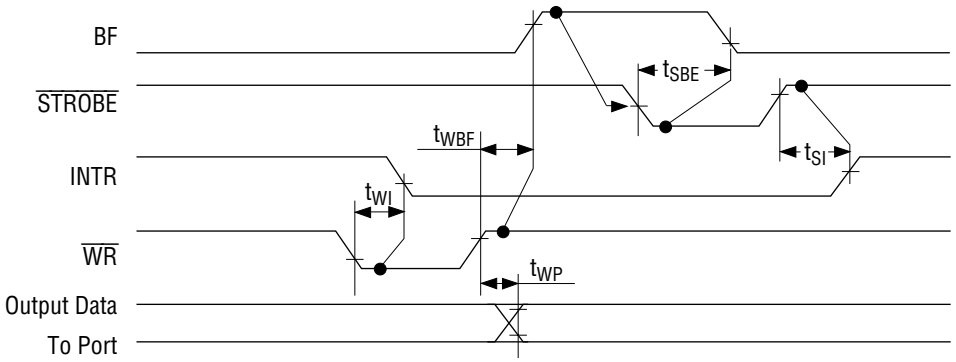
Write Cycle



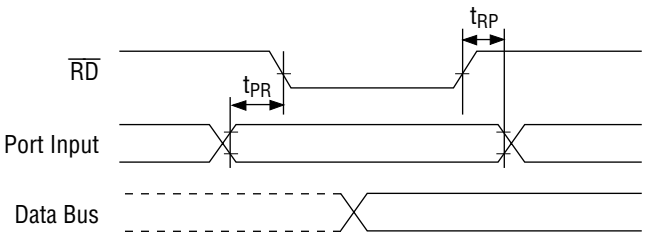
Strobe Input Mode



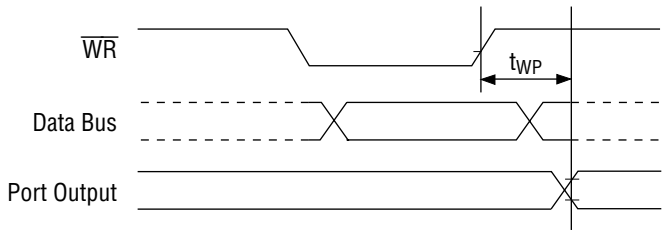
Strobe Output Mode



Basic Input Mode

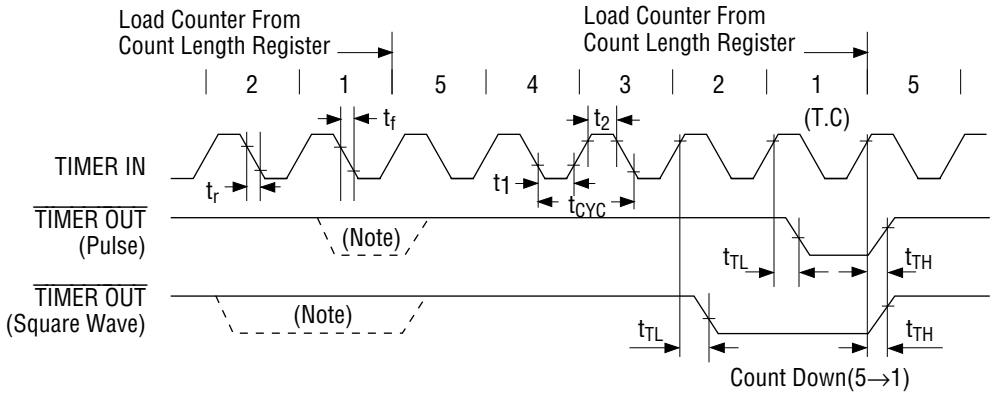


Basic Output Mode



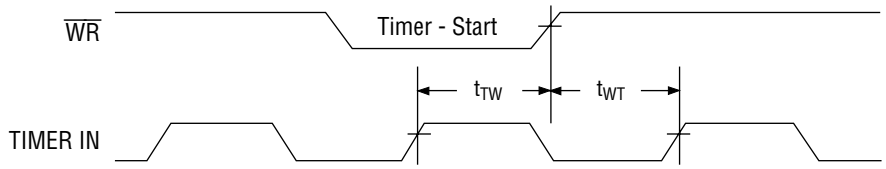
Note: The DATA BUS timing is the same as the read and write cycles.

Timer Waveforms 1



Note: Periodically outut according to the output mode (m1=1) programming contents.

Timer Waveforms 2

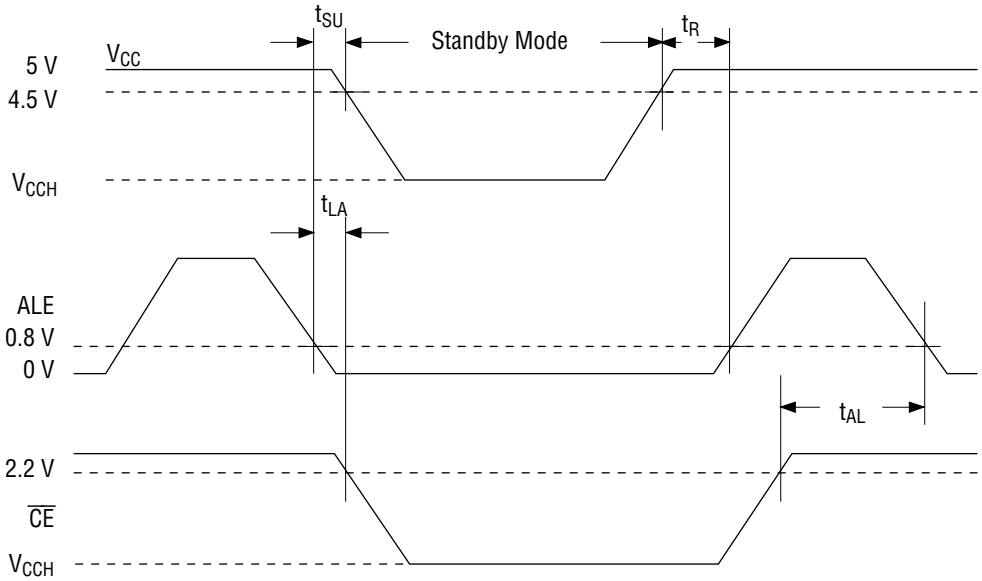


RAM DATA HOLD CHARACTERISTICS AT LOW SUPPLY VOLTAGE

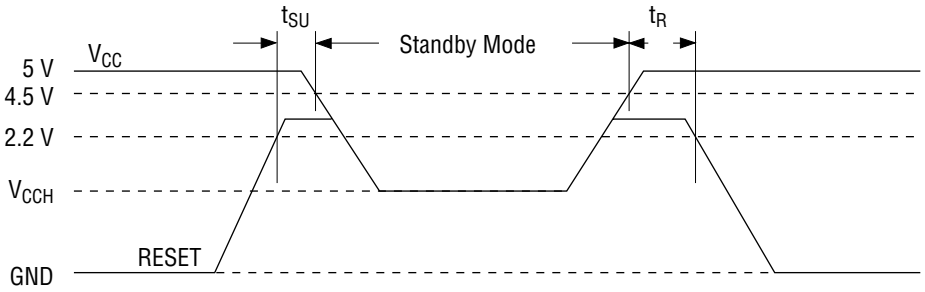
Item	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Data Holding Supply Voltage	V_{CCH}	V_{IN} = 0 V or V_{CC}, ALE = 0 V	2.0	—	—	V
Data Holding Supply Current	I_{CCH}	$V_{CC} = V_{CCH}$, ALE = 0 V_{IN} = 0 V or V_{CC}	—	0.05	20	µA
Setup Time	t_{SU}		30	—	—	ns
Hold Time	t_R		20	—	—	ns

Two ways to place device in standby mode:

(1) Method using $\overline{CE}$



(2) Method using RESET



Note: In this case, the C/S register is reset, the port is set into the input mode, and the timer stops.

PIN FUNCTION

Symbol	Function
RESET	A high level input to this pin resets the chip, places all three I/O ports in the input mode, resets all output latches and stops timer.
ALE	Negative going edge of the ALE (Address Latch Enable) input latches AD_{0-7}, IO/$\overline{M}$, and $\overline{CE}$ signals into the respective latches.
AD_{0-7}	Three-state, bi-directional address/data bus. Eight-bit address information on this bus is read into the internal address latch at the negative going edge of the ALE. Eight bits of data can be read from or written to the chip using this bus depending on the state of the WRITE or READ input.
$\overline{CE}$	When the $\overline{CE}$ input is high, both read and write operations to the chip are disabled.
IO/$\overline{M}$	A high level input to this pin selects the internal I/O functions, and a low level selects the memory.
$\overline{RD}$	If this pin is low, data from either the memory or ports is read onto the AD_{0-7} lines depending on the state of the IO/$\overline{M}$ line.
$\overline{WR}$	If this pin is low, data on lines AD_{0-7} is written into either the memory or into the selected port depending on the state of the line IO/$\overline{M}$ line.
PA_{0-7} (PB_{0-7})	General-purpose I/O pins. Input/output directions can be determined by programming the command/ status (C/S) register.
PC_{0-5}	Three pins are usable either as general-purpose I/O pins or control pins for the PA and PB ports. When used as control pins, they are assigned to the following functions: PC_0: A INTR (port A interrupt) PC_1: $\overline{A\ BF}$ (port A full) PC_2: $\overline{A\ STB}$ (port A strobe) PC_3: B INTR (port B interrupt) PC_4: $\overline{B\ BF}$ (port B buffer full) PC_5: $\overline{B\ STB}$ (port B strobe)
TIMER IN	Input to the counter/timer
$\overline{TIMER\ OUT}$	Timer output. When the present count is reached during timer operation, this pin provides a square-wave or pulse output depending on the programmed control status.
V_{CC}	3–6V power supply
GND	GND

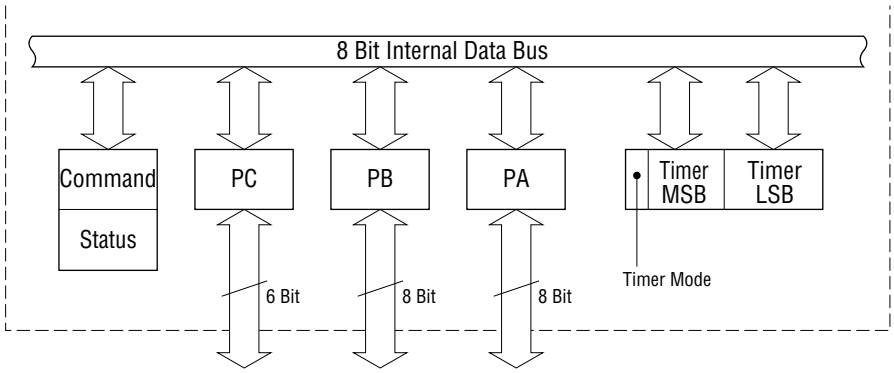
OPERATION

Description

The MSM81C55-5 has three functions as described below.

- 2K-bit static RAM (256 words × 8 bits)
- Two 8-bit I/O ports (PA and PB) and a 6-bit I/O port (PC)
- 14-bit timer counter

The internal register is shown in the figure below, and the I/O addresses are described in the table below.

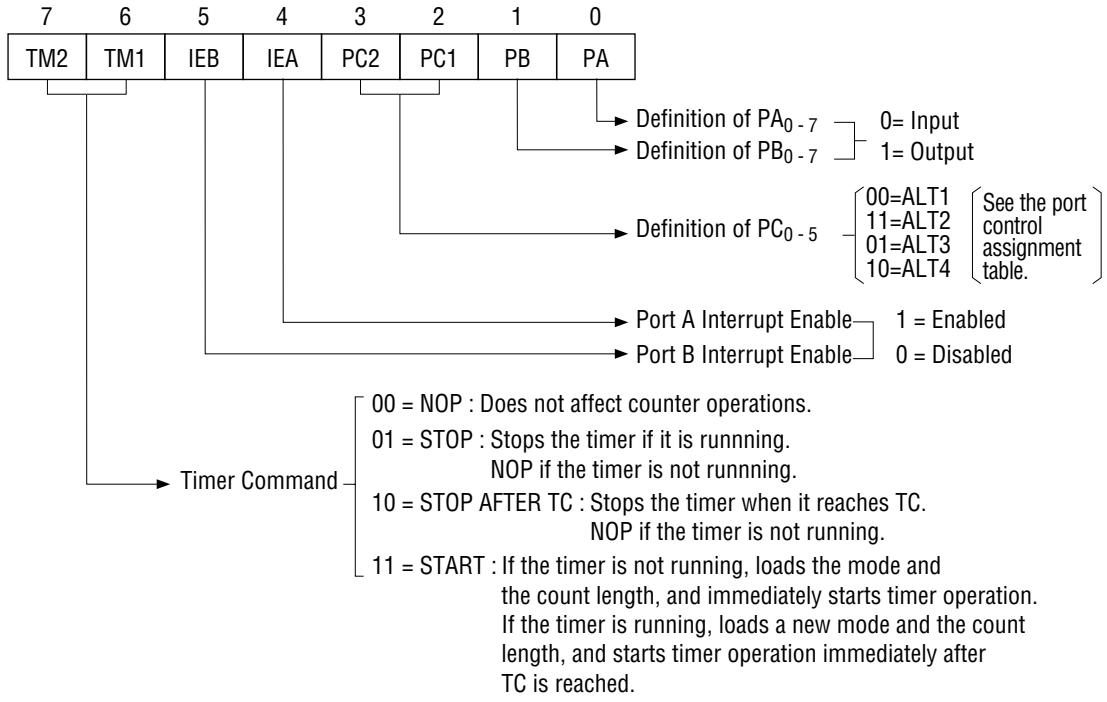


I/O Address								Selecting Register
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
×	×	×	×	×	0	0	0	Internal command/status register
×	×	×	×	×	0	0	1	Universal I/O port A (PA)
×	×	×	×	×	0	1	0	Universal I/O port B (PB)
×	×	×	×	×	0	1	1	I/O port C (PC)
×	×	×	×	×	1	0	0	Timer count lower position 8 bits (LSB)
×	×	×	×	×	1	0	1	Timer count upper position 6 bits and timer mode 2 bits (MSB)

×: Don't care.

(1) Programming the Command/Status (C/S) Register

The contents of the command register can be written during an I/O cycle by addressing it with an I/O address of xxxxx000. Bit assignments for the register are shown below:

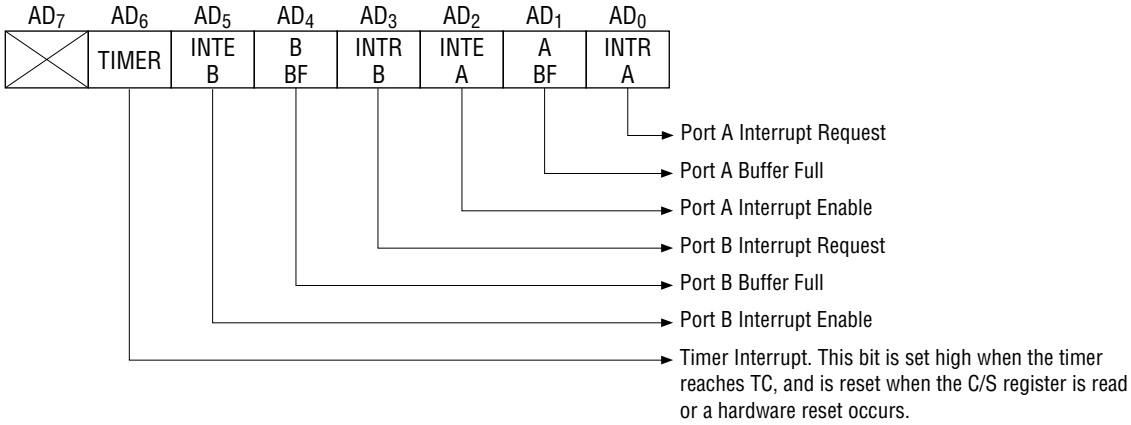

7 6 5 4 3 2 1 0
TM2 TM1 IEB IEA PC2 PC1 PB PA
Definition of PA0 - 7
Definition of PB0 - 7
0= Input
1= Output
Definition of PC0 - 5
00=ALT1
11=ALT2
01=ALT3
10=ALT4
See the port control assignment table.
Port A Interrupt Enable
Port B Interrupt Enable
1 = Enabled
0 = Disabled
Timer Command
00 = NOP : Does not affect counter operations.
01 = STOP : Stops the timer if it is runnning.
NOP if the timer is not runnning.
10 = STOP AFTER TC : Stops the timer when it reaches TC.
NOP if the timer is not running.
11 = START : If the timer is not running, loads the mode and the count length, and immediately starts timer operation.
If the timer is running, loads a new mode and the count length, and starts timer operation immediately after TC is reached.

Port Control Assignment Table

Pin	ALT1	ALT2	ALT3	ALT4
PC_0	Input port	Output port	A INTR	A INTR
PC_1	Input port	Output port	A BF	A BF
PC_2	Input port	Output port	A STB	A STB
PC_3	Input port	Output port	Output port	B INTR
PC_4	Input port	Output port	Output port	B BF
PC_5	Input port	Output port	Output port	B STB

(2) Reading the C/S Register

The I/O and timer status can be accessed by reading the contents of the Status register located at I/O address xxxxx000. The status word format is shown below:


AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
TIMER
INTE B
B BF
INTR B
INTE A
A BF
INTR A
Port A Interrupt Request
Port A Buffer Full
Port A Interrupt Enable
Port B Interrupt Request
Port B Buffer Full
Port B Interrupt Enable
Timer Interrupt. This bit is set high when the timer reaches TC, and is reset when the C/S register is read or a hardware reset occurs.

(3) PA and PB Registers

These registers may be used as either input or output ports depending on the programmed contents of the C/S register. They may also be used either in the basic mode or in the strobe mode.

I/O address of the PA register: xxxxx001

I/O address of the PB register: xxxxx010

(4) PC Register

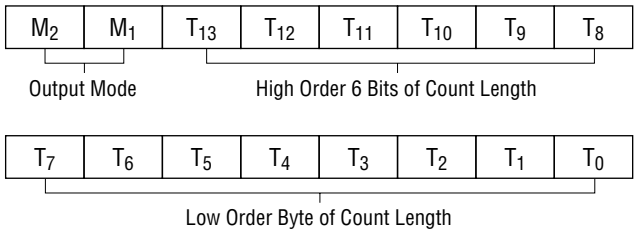
The PC register may be used as an input port, output port or control register depending on the programmed contents of the C/S register. The I/O address of the PC register is xxxxx011.

(5) Timer

The timer is a 14-bit down counter which counts TIMER IN pulses.

The low order byte of the timer register has an I/O address of xxxxx100, and the high order byte of the register has an I/O address of xxxxx101.

The count length register (CLR) may be preset with two bytes of data. Bits 0 through 13 are assigned to the count length and bits 14 and 15 specify the timer output mode. A read operation of the CLR reads the contents of the counter and the pertinent output mode. The initial value range which can initially be loaded into the counter is 2 through 3FFF hex. Bit assignments to the timer counter and possible output modes are shown in the following.



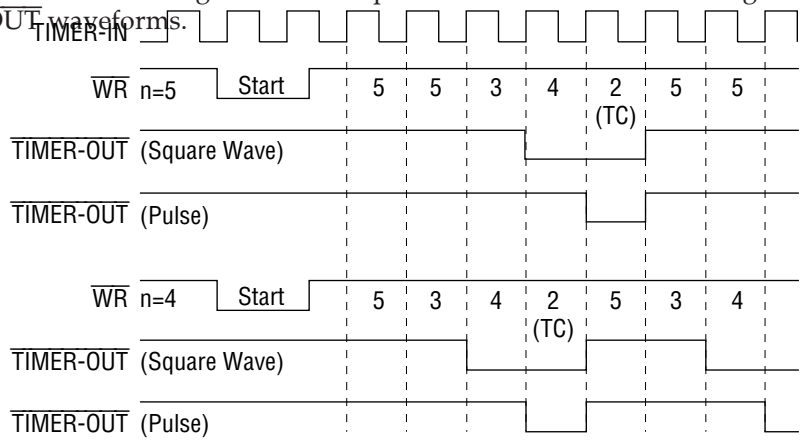
M_2	M_1	
0	0	Outputs a low-level signal in the latter half (Note 1) of a count period.
0	1	Outputs a low-level signal in the latter half of a count period, automatically loads the programmed count length, and restarts counting when the TC value is reached.
1	0	Outputs a pulse when the TC value is reached.
1	1	Outputs a pulse each time the preset TC value is reached, automatically loads the programmed count length, and restarts from the beginning.

Notes: 1. When counting an asymmetrical value such as (9), a high level is output during the first period of five,and a low level is output during the second period of four.
2. If an internal counter of the MSM81C55-5 receives a reset signal, count operation stops but the counter is not set to a specific initial value or output mode. When restarting count operation after reset, the START command must be executed again through the C/S register.

Note that while the counter is counting, you may load a new count and mode into the CLR. Before the new count and mode will be used by the counter, you must issue a START command to the counter. Please note the timer circuit on the MSM81C55-5 is designed to be a square-wave timer, not a event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulse received. After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulse required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order.

1. STOP the counter
2. Read in the 16-bit value from the count registers.
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count-1 if full count is odd).

Note: If you started with an odd count and you read the count registers before the third count pulse occurs, you will not be able to recognize whether one or two counts have occurred. Regardless of this, the MSM81C55-5 always counts out the right number of pulses in generating the TIMER OUT waveforms.



Note: n is the value set in the CLR. Figures in the diagram refer to counter values

(6) Standby Mode (see page 7)

The MSM81C55-5 is placed in standby mode when the high level at the $\overline{CE}$ input is latched during the negative going edge of ALE. All input ports and the timer input should be pulled up or down to either V_{CC} or GND potential.

When using battery back-up, all ports should be set low or in input port mode. The timer output should be set low. Otherwise, a buffer should be added to the timer output and the battery should be connected to the power supply pins of the buffer.

By setting the reset input to a high level, the standby mode can be selected. In this case, the command register is reset, so the ports automatically set to the input mode and the timer stops.

NOTICE ON REPLACING LOW-SPEED DEVICES WITH HIGH-SPEED DEVICES

The conventional low speed devices are replaced by high-speed devices as shown below.
When you want to replace your low speed devices with high-speed devices, read the replacement notice given on the next pages.

High-speed device (New)	Low-speed device (Old)	Remarks
M80C85AH	M80C85A/M80C85A-2	8bit MPU
M80C86A-10	M80C86A/M80C86A-2	16bit MPU
M80C88A-10	M80C88A/M80C88A-2	8bit MPU
M82C84A-2	M82C84A/M82C84A-5	Clock generator
M81C55-5	M81C55	RAM.I/O, timer
M82C37B-5	M82C37A/M82C37A-5	DMA controller
M82C51A-2	M82C51A	USART
M82C53-2	M82C53-5	Timer
M82C55A-2	M82C55A-5	PPI

Differences between MSM81C55-5 and MSM81C55

1) Manufacturing Process

These devices use a 3 µ Si-CMOS.

2) Design

These devices use the same chip. However, different outgoing inspection standards are used for these devices separately.

3) Electrical Characteristics

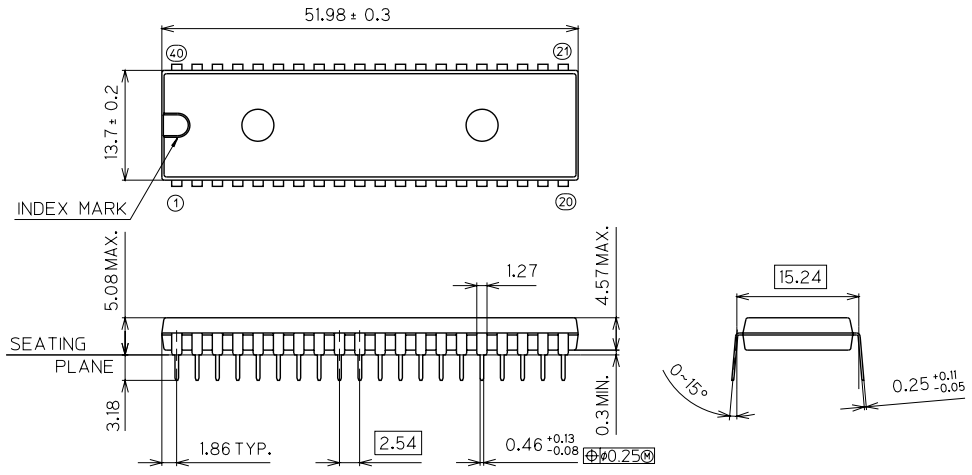
"Oki's '96 Data Book for MICROCONTROLLER" describes that the MSM81C55-5 satisfies the electrical characteristics of the MSM81C55.

As shown above, the devices can be replaced without any trouble.

PACKAGE DIMENSIONS

(Unit : mm)

DIP40-P-600-2.54



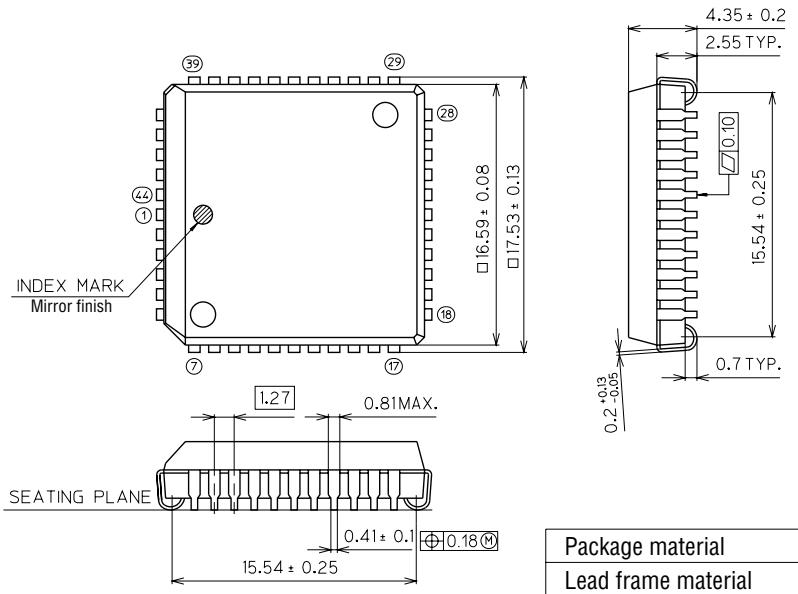
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.10 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFJ44-P-S650-1.27



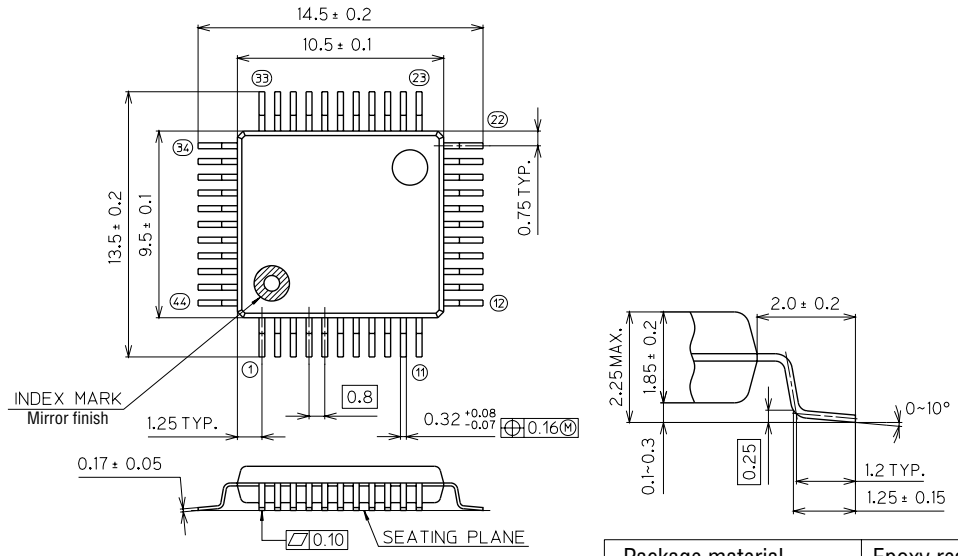
Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	2.00 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).